ABSTRACT

A dual-gate field effect transistor includes a substrate 1, a source 7-1, a drain 7-2, a vertical channel 5 provided between the source and the drain as rising from the substrate, a pair of gate insulation films 6-1 and 6-2 sandwiching the channel from a direction orthogonal to a carrier-running direction in the channel and a pair of gate electrodes 3-1 and 3-2 facing the vertical channel 5, respectively, via the pair of gate insulation films 6-1 and 6-2, wherein the pair of insulation films have different thicknesses t1 and t2. It is also possible that the pair of gate insulation films 6-1 and 6-2 have different permittivities $\varepsilon 1$ and $\varepsilon 2$ and that the pair of gate electrodes have different work functions $\Phi 1$ and $\Phi 2$. Thus, it is possible to set the threshold voltage of the dual-gate field effect transistor to a desired value when fabricating it. Furthermore, it is possible to avoid the problem of an increase in subthreshold slope that occurs in the prior art.